CLAIMS

1. A semiconductor memory device comprising:

a first data holding circuit specified by driving a control line and a first data supply line;

a second holding circuit specified by driving the control line and a second data supply line and provided at a position adjacent to the first data holding circuit;

a comparison circuit for detecting an output level of the second data holding circuit and generating a timing signal in accordance with a result of comparison between this detection result and a threshold voltage; and

a drive circuit for driving the first control line in accordance with the timing signal of the comparator when reading the data from the first data holding circuit.

2. A semiconductor memory device as set forth in claim 1, wherein said control line is a word line and said first and second data supply lines are bit lines.

3. A semiconductor memory device as set forth in claim 1, further comprising a control circuit for deactivating a control line by said drive circuit in accordance with a timing signal of said comparision circuit and precharging to set the bias of said second data holding circuit to a predetermined level.

4. A semiconductor memory device as set forth in claim 1, providing said second data holding circuit for

each said first data holding circuit.

5. A semiconductor memory device comprising:

a first data holding circuit specified by driving a first control line and a first data supply line;

a second holding circuit specified by driving a second control line and a second data supply line and provided at a position adjacent to the first data holding circuit;

a first comparison circuit for detecting an output level of the second data holding circuit and generating a timing signal in accordance with a result of comparison between this detection result and a threshold voltage;

a first drive circuit for driving the first control line in accordance with the timing signal of the first comparator when reading the data from the first data holding circuit;

a second comparison circuit for detecting the level of the second control line, comparing this detection result and the threshold voltage, and generating a second timing signal in accordance with the result; and

a second drive circuit for driving the second control line in accordance with the timing signal of the second comparator when reading the data from the first data holding circuit.

6. A semiconductor memory device as set forth in claim 5, wherein said first and second control lines are word lines and said first and second data supply lines are bit lines.

7. A semiconductor memory device as set forth in claim 5, further comprising a control circuit for deactivating a control line by said drive circuit in accordance with a timing signal of said first comparision circuit and precharging to set the bias of said second data holding circuit to a predetermined level.

8. A semiconductor memory device as set forth in claim 5, providing said second data holding circuit in a row direction and column direction of said first data holding circuit.

9. A semiconductor memory device having:

a first memory cell connected to a word line and a pair of first bit lines,

a second memory cell connected to the word line and a pair of second bit lines, and

a word line driver activating at least the word line at a common timing and

determining the timing of the reading of the data in accordance with the level of the second bit line connected to the second memory cell when data is read out from the first memory cell, wherein

the word line driver deactivates at least the word line connected to the second memory cell and precharges the second bit line connected to the second memory cell to the predetermined potential when the voltage difference of the pair of second bit lines becomes a previously set value.

10. A semiconductor memory device as set forth in claim 9, wherein said word line driver includes a comparator unit connected to said pair of second bit lines and comparing the potentials of the pair of second bit lines, a word line control unit for deactivating the word line connected to at least the second memory cell when the potential difference of said pair of second bit lines becomes a previously set value as a result of the comparison by said comparator unit, and a precharge circuit for precharging the pair of second bit lines connected to the second memory cell to a predetermined potential when the word line connected to the said memory cell is deactivated by said word line control unit.

11. A semiconductor memory device as set forth in claim 9, wherein:

said word line has said first memory cell, said second memory cell, and said word line driver connected in common to it, and

said word line driver activates said word line

at a common timing, deactivates said word line connected to said first and second memory cell when the potential difference of said pair of second bit lines becomes a previously set value, and precharges said second bit line connected to said second memory to a predetermined potential.

12. A semiconductor memory device comprising:

a first memory cell connected to a word line and a pair of first bit lines;

a sense amplifier connected to the first bit lines;

a first precharge circuit for precharging the first bit lines to a predetermined potential;

a second memory cell connected to the word line and a pair of second bit lines;

a first comparator unit for comparing potentials of the pair of second bit lines and generating a timing signal when the voltage difference becomes a previously set value;

a word line driver connected to the word line and the pair of second bit lines and precharging the second bit lines to the predetermined potential based on at least the potential of the word line; and

a control circuit for making the word line driver activate the word line in a state where the first

bit lines and the second bit lines are precharged to discharge the first bit lines and the second bit lines, making the sense amplifier detect the voltage difference of the first bit lines based on the timing signal output from the first comparator unit when the voltage difference of the pair of second bit lines becomes the previously set value, and making the first precharge circuit precharge the first bit lines to the predetermined potential, wherein

the word line driver includes:

a second comparator unit for comparing the potentials of the pair of second bit lines and generating the timing signal when the voltage difference becomes the previously set value,

a word line control unit for deactivating the word line connected to the second memory cell based on at least the timing signal generated by the second comparator unit, and

a second precharge circuit for precharging the pair of second bit lines connected to the second memory cell to a predetermined potential when the word line becomes deactive.

13. A semiconductor memory device comprising:

a first memory cell connected to a first word line and a pair of first bit lines;

a sense amplifier connected to the first bit

lines;

a first precharge circuit for precharging the first bit lines to a predetermined potential;

a first word line driver connected to the first word line and activating and deactivating the first word line;

a second memory cell connected to the second word line and a pair of second bit lines;

a first comparator unit for comparing the potentials of the pair of second bit lines and generating a timing signal when the voltage difference becomes the previously set value;

a second word line driver connected to the second word line and the pair of second bit lines and precharging the second bit lines to the predetermined potential based on the potential of at least the second word line; and

a control circuit for making the word line driver activate the word line in a state where the first bit lines and the second bit lines are precharged to discharge the first bit lines and the second bit lines, making the sense amplifier detect the voltage difference of the first bit lines based on the timing signal output from the first comparator unit when the voltage difference of the pair of second bit lines becomes the previously set

value, and making the first precharge circuit precharge the first bit lines to the predetermined potential, wherein

the second word line driver includes:

a second comparator unit for comparing the potentials of the pair of second bit lines and generating the timing signal when the voltage difference becomes the previously set value,

a word line control unit for deactivating the second word lines connected to the second memory cell based on the timing signal generated by at least the second comparator unit, and

a second precharge circuit for precharging the pair of second bit lines connected to the second memory cell to the predetermined potential when the second word line becomes deactive.

14. A reading method of a semiconductor memory device having a first memory cell connected to a word line and a pair of first bit lines, a second memory cell connected to a word line and a pair of bit lines, and a word line driver deactivating at least the word line at a common timing, wherein

when the data is read out from the first memory cell, the timing of reading of the data is determined in accordance with the level of the second bit lines connected to the second memory cell, and

when the voltage difference of the pair of second bit lines becomes the previously set value, the word line driver deactivates at least the word line connected to the second memory cell to precharge the second bit lines connected to the second memory cell to the predetermined potential.

15. A reading method of a semiconductor memory device as set forth in claim 14, further comprising having a comparator unit in said word line driver connected to said pair of second bit lines compare the potentials of the pair of second bit lines, having a word line control unit in said word line driver connected to said second memory cell deactivate said word line when the potential difference of said pair of second bit lines becomes a previously set value as a result of the comparison by said comparator unit, and having a precharge circuit in said word line driver precharge the pair of second bit lines connected to the second memory cell to a predetermined potential when the word line connected to the second memory cell is deactivated by said word line control unit.

16. A reading method of a semiconductor memory device as set forth in claim 14, further having said word line have said first memory cell, said second memory cell, and said word line driver connected in common to it, and having said word line driver activate said word line at a

common timing, deactivate said word line connected to said first and second memory cell when the potential difference of said pair of second bit lines becomes a previously set value, and precharge said second bit line connected to said second memory to a predetermined potential.